MMIC Power amplifiers and LNAs in 100-nm GaN on SiC European technology for Q/V band VHTS and constellations.

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Abstract

Semiconductors are critical to the national security of the European member states and to the functioning of the European economy. III-V semiconductors like gallium nitride (GaN) are particularly of interest for space and telecom applications due to the very high efficiency of these materials. The European project SGAN-Next is focused on developing a European GaN on SiC MMIC process for high frequency operating devices (Q band and beyond) targeting flexible payloads for LEO/GEO applications. In this paper, first designs of a medium (2W and 5W) and high-power amplifier (10W) for Q-band, as well as low noise amplifiers at V-band are presented.

INTRODUCTION

Among the different technologies that can improve space payloads and mission's performances, the use of GaN has attracted considerable attention in the last years [1-5]. GaN technology has been key enabler for advanced active antennas. The evolution of this technology toward higher frequencies will allow increasing satellite data capacity and the integration of compact payloads, which is essential for future VHTS and constellations. This contribution is within the framework of the European SGAN-Next project, whose main objective is to develop a European 100-nm GaN on SiC MMIC process for high frequency operating devices (Q band and beyond) targeting flexible payloads for LEO/GEO applications and demonstrate outstanding performance with the design of MMICs with power amplifier, LNA and T/R switch functions. These circuits will be space-qualified during the program.

Space systems have rapidly evolved in the past years from fixed GEO platforms with a limited number of transponders to high capacity and flexible satellites in GEO together with large constellations in LEO orbits. Both LEO and GEO applications require flexible antenna systems that can generate several beams with multi-Gigabit capacity and perform beam steering to adapt the capacity to the geographical demand. Focussing on the power amplification function of the mm-wave front end, these systems are based on phase arrays that require efficient SSPA's to optimize the use of the available power from solar panels and avoid thermal dissipation issues. GaN has proven to be the best technology for these systems up to Ku/K band, displacing the use of TWTAs, but the performance at Q-band and beyond of existing processes are still under development to meet system requirements.

Different MMICs have been designed, and they are currently under fabrication based on the 100-nm GaN on SiC UMS technology (GH10-10). The proposed MMICs can be classified in three different categories: 7/10-W level Power Amplifiers (PA) for GEO applications at Q band (37.5 – 42.5 GHz), 3-W level Medium Power Amplifier (MPA) for LEO applications at Q band, and robust Low Noise Amplifiers (LNA) at V band (47.5 – 52.5 GHz).

2W MEDIUM POWER MMIC AMPLIFIER FOR Q-BAND OPERATION

This is a three-stage amplifier, where the transistor sizes are 6×50 μm in the first stage, 2×6×50 μm in the second stage, and 4×6×60 μm in the third stage.

At the input of each transistor, a series RC parallel structure is used as a stabilization network to prevent gain at low frequencies. The structure consists of a first transistor that increases the power to a sufficient level, followed by an output split into two transistors, which further split into the final four transistors of the last stage. All gate voltages are -2.5 V, and drain voltages are 14 V, resulting in a quiescent current of approximately 25 mA per transistor.
The final stage features a 4-to-1 reactive combiner. When dealing with wide bandwidths, the reactive combiner is designed with all branches balanced relative to each other. Throughout the MMIC, symmetry is maintained along the X-axis to prevent imbalances and potential oscillations. Stage-to-stage matching is performed from complex impedance to complex impedance.

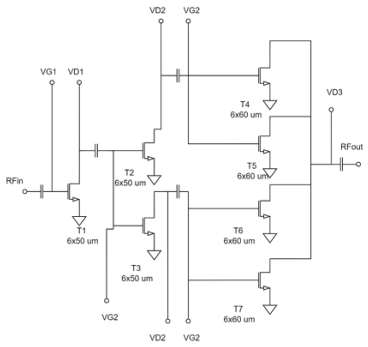

Fig. 1. Schematic diagram for the 2W Medium-power MMIC amplifier.

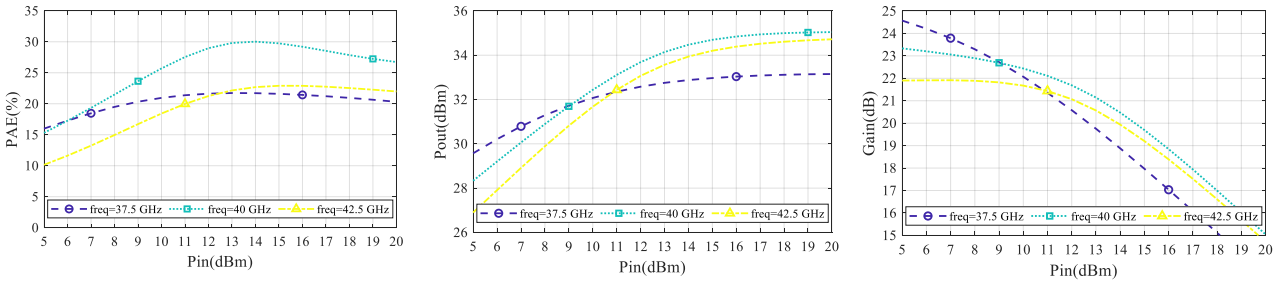

Fig. 2. PAE, Pout and gain versus the input power.

The large-signal simulated results can be seen in Fig. 2. The maximum PAE is achieved for an input power of 13 dBm, where the PAE is greater than 20% at 5 GHz, with an output power exceeding 32.7 dBm, a gain over 19.5 dB, and a power consumption above 8.5 W. The small-signal simulation is shown in Fig. 3. As can be seen, S11 is lower than -7.8 dB, and S22 is lower than -9.5 dB. Regarding S21, it remains greater than 20 dB across the entire band. The reactive combiner-type structure exhibits good performance within the design bandwidth.

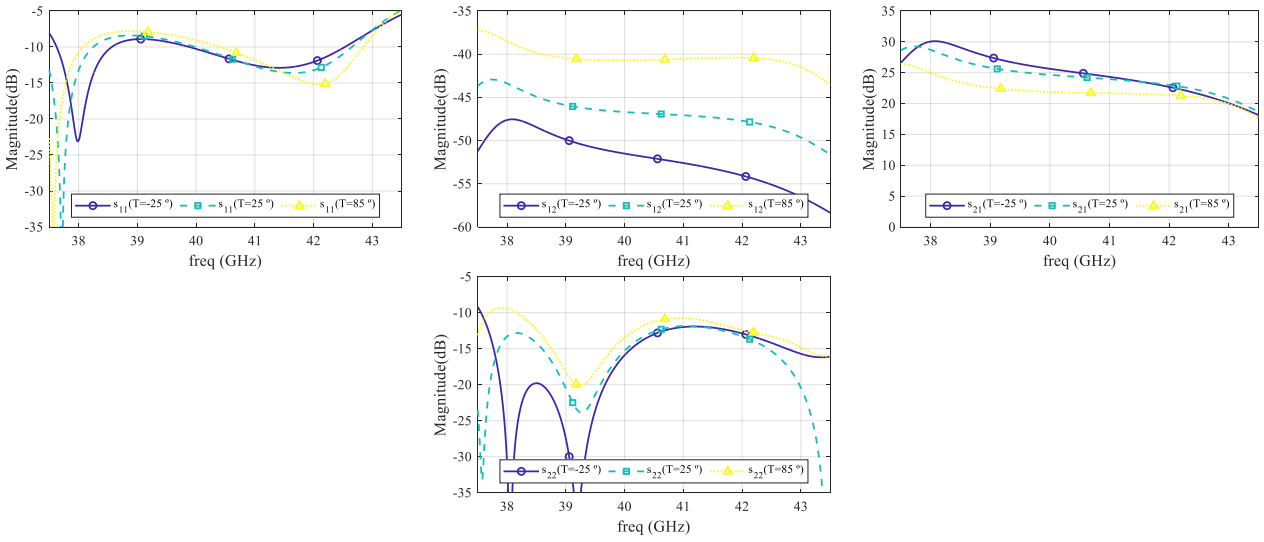

Fig. 3. S-Parameters simulation at different room temperatures.

5W MEDIUM POWER MMIC AMPLIFIER FOR Q-BAND OPERATION

Since the technology is still in an early stage, a simple topology has been chosen for implementation. Fig. 4 presents a block diagram that details the topology of the MPA, implemented in an area of 5 mm × 3 mm. The input quadrature hybrid splits the incoming signal, introducing a 90-degree phase shift between the branch inputs. Both branches are identical and consist of two stages. The first stage is composed of a single transistor with 8 fingers of 100 µm, which drives a second stage made up of two transistors with 8 fingers of 100 µm, combined using Wilkinson power dividers. Finally, both signals are recombined in phase through the output hybrid.

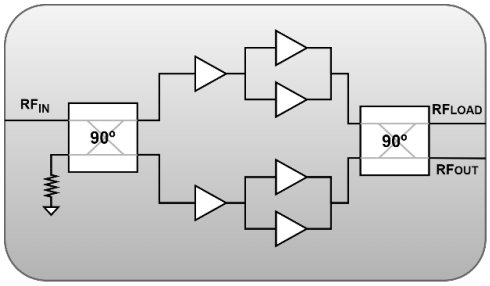

Fig. 4. 5W MPA Block Diagram.

After analyzing the optimal impedances of the transistor array in the GH10 process, the TZ variant with 8 fingers and a gate width of 100 µm was selected. This device was biased to achieve maximum PAE. With a drain voltage, V_D, of 15 V and a quiescent current, I_Q, of 49.8 mA, obtained when applying a gate voltage, V_G, of -2.6 V, the transistor reaches a PAE of 34.2%, delivering a maximum gain of 7.6 dB and an output power of 31.98 dBm under the maximum PAE condition with an input power of 26 dBm.

To stabilize the transistor, a series RC network connected to ground has been implemented as close as possible to its input. This ensures unconditional stability within the range where the transistor exhibits gain. Additionally, the gate bias networks help to improve low-frequency stability. To confirm that the MPA is stable, stability analyses focused on this type of device have been conducted. Within the operating band (37.5 – 42.5 GHz), the design aims to achieve the nominal power of 3 W with the highest possible PAE. As shown in Fig. 5, within this band, the MPA delivers 3.5 W with a maximum PAE of 20.6% for an input power of 31 dBm. The maximum gain is 9.5 dB, with a power consumption of 22.5 W, reaching a saturation power of 5 W.

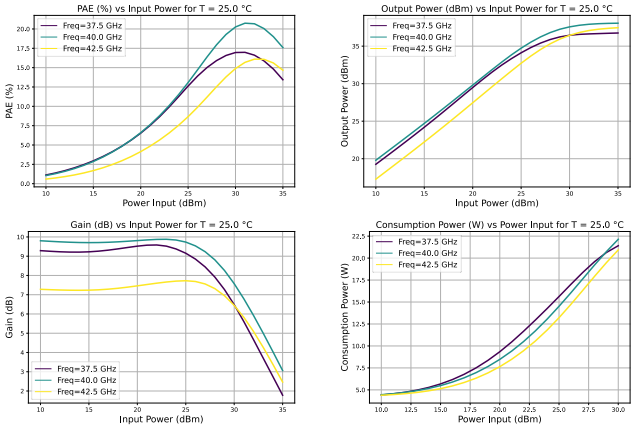

Fig. 5. Large Signal 5 W MPA performance.

In the small-signal representation Fig. 6, the effects of the quadrature hybrids are reflected. The S_{11} and S_{22} parameters, despite the slight impedance variations of the transistors due to the temperature at the MMIC base, remain below -20 dB and -28 dB, respectively.

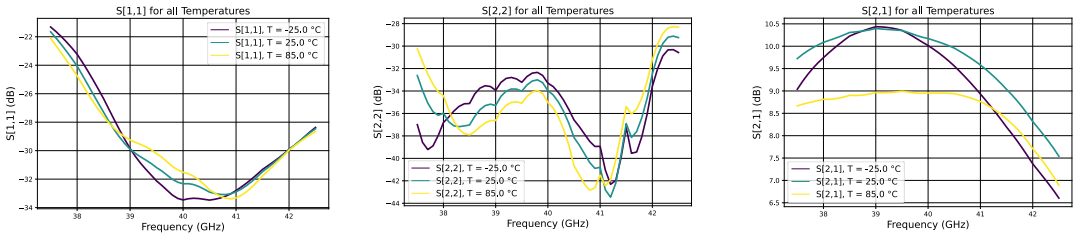

Fig. 6. Small-Signal 5W MPA performance.

7W/12W HIGH POWER MMIC AMPLIFIER FOR Q-BAND OPERATION

Two different designs for the high-power operation are presented. First, A MMIC PA was designed with 7 W saturated output power across the frequency band: the PA features minimum 28% PAE close to saturation with 13 dB associated gain. At 3.2dB OBO, the PA meets the NPR = 15 dB linearity requirement with PAE = 21% and associated gain of 19 dB. The PA is a three-stage circuit with a combination of eight 8x50 µm HEMTs in the final stage for total active periphery of 3.2 mm. Each HEMT is made unconditionally stable with a RC stabilizing network at the gate. The MMIC size is 4.2 mm x 4 mm, and its simulated performance is provided in Fig. 7.

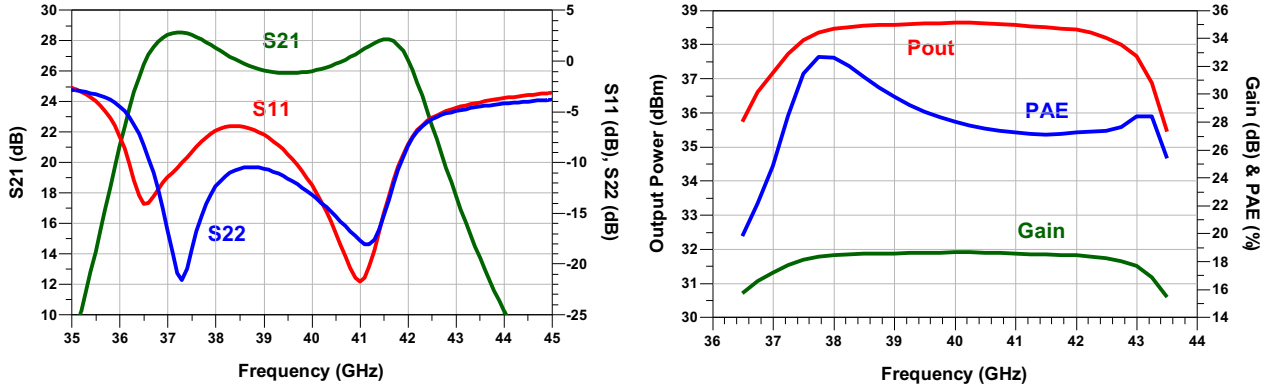

Fig. 7. (Left) Small-signal performance of the 7W PA MMIC. (Right) Large-signal performance of the 7W PA MMIC at saturation.

Moreover, a second design is provided based on the 5 W design from Fig. 4 but increasing the number of transistors per stage and using low-impedance dividers instead of the Wilkinson dividers. The total size in this case is 5 mm × 4 mm. Throughout the design process, the same criteria applied to the 5 W design were followed. The transistor with 8 fingers and a 100 µm gate width is ideal for this application, where maximizing output power is the primary goal. To ensure efficiency is maintained, the biasing conditions and optimal impedances from the first design are preserved. In Fig. 8, it is shown that within the operating band (37.5 – 42.5 GHz), the HPA delivers 9 W with a maximum PAE of 20.2% and a power consumption of 40 W. It can achieve a maximum output power under saturation of 12 W. The maximum gain of the MMIC is 10.3 dB.

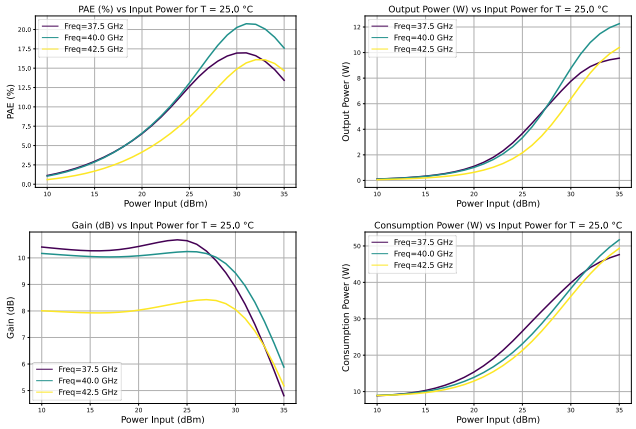

Fig. 8. Large Signal 10 W HPA performance.

The small-signal results are depicted in Fig. 9, for the input matching are similar to those observed in the previous design, as the topology is maintained. The S_{11} and S_{22} parameters, regardless of the HPA's base temperature, exhibit levels below -25 dB.

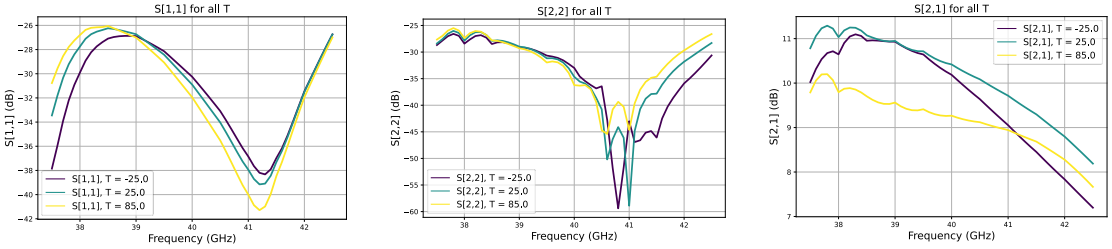

Fig. 9. Small-Signal 10 W HPA performance.

LOW NOISE MMIC AMPLIFIER FOR V-BAND OPERATION

For the design of the LNA at V-Band, two different configurations of transistor have been used, TZ and ISV. The main difference is that source degradation is allowed in the TZ configuration. First analysis of both transistors shows a better performance for the TZ in terms of noise figure, and better gain performance for the ISV configuration. In both cases, to have a good compromise between noise figure and gain, a density current of 75mA/mm is considered. Both configurations are based on a three-stage architecture to achieve a total gain G > 20 dB using 4x50um transistors. The schematic block diagrams are shown in Fig. 10.

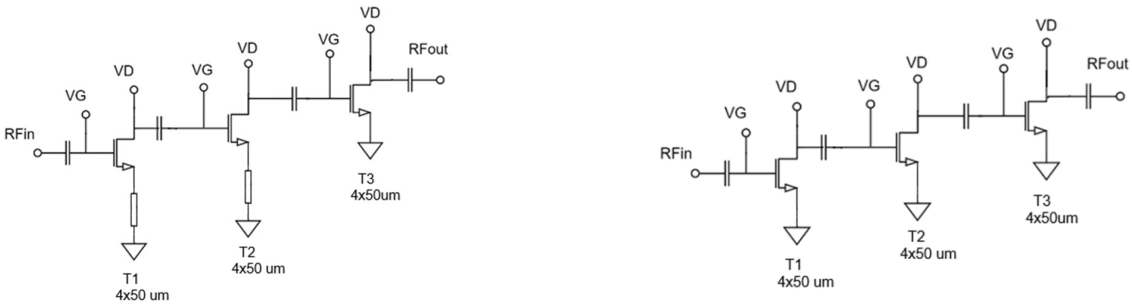

Fig. 10. General schematic diagram for (Left) the LNA based on TZ transistors and (Right) LNA based on ISV transistors.

The total size is 4,2x1,7 mm for both designs. A resistor was used in the gate bias supply to limit the DC gate current, along with another in parallel with a capacitor to enhanced transistor stability. The current density used for each stage is 75 mA/mm. The simulated results for the ISV and TZ configurations are shown in Fig. 11 and Fig. 12 respectively in the range of 47 to 52 GHz. In general terms, the behavior in terms of noise figure is better for the TZ configuration due to the possibility to degenerate the source by means of inductances to ground. Moreover, in terms of gain, although the gain peak is higher with the ISV configuration as expected, the TZ provides a flatter response in the specific bandwidth.

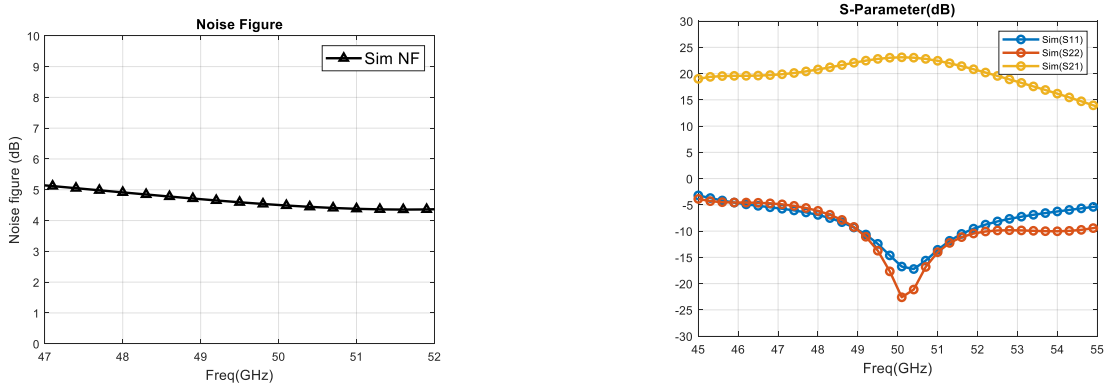

Fig. 11. Noise Figure and S-Parameters simulation for the ISV configuration.

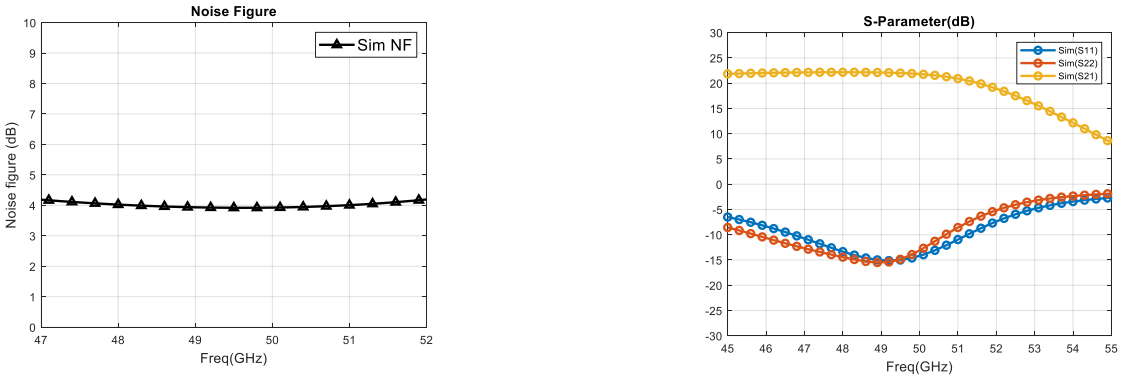

Fig. 12. Noise Figure and S-Parameters simulation for the TZ configuration.

CONCLUSIONS

With the aim to evaluate a European GaN on SiC MMIC process for high frequency operating devices (Q-band and beyond) targeting flexible payloads for LEO/GEO applications, several designs under fabrication are presented. Two medium-power amplifiers with 2W and 5W output power, two high-power amplifiers with 7W and 12W output power at Q-band, and two low-noise amplifiers with noise figure below 5dB and gain above 20dB for V-band operation. At a simulation level, the performance of the amplifiers complies with different specifications in terms of output power, gain, linearity and noise figure among others.

ACKNOWLEDGEMENT

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REFERENCES

[1] C. Ramella, C. Florian, E. Cipriani, M. Pirola, F. Giannini and P. Colantonio, "*Ka-band 4 W GaN/Si MMIC power amplifier for CW radar applications*," *2020 15th EuMIC*, 2021, pp. 33-36, doi: 10.1109/EuMIC48047.2021.00020.

[2] J. Moron et al, "*12W, 30% PAE, 40 GHz power amplifier MMIC using a commercially available GaN/Si process*," 2018 IEEE/MTT-S IMS, 2018, pp. 1457-1460, doi: 10.1109/MWSYM.2018.8439689.

[3] R. Giofrè, F. Costanzo and E. Limiti, "*Q-Band MMIC High Power Amplifiers for High Throughput Satellites in GaN-on-Si Technology*," 2019 IEEE APMC, 2019, pp. 1044-1046, doi: 10.1109/APMC46564.2019.9038504.

[4] P. Feuerschütz *et al*., "*Two Q-band power amplifier MMICs in 100 nm AlGaN/GaN HEMT technology*," *2018 11th GeMiC*, 2018.

[5] C. Han and H. Tao, "*A 18-40GHz 10W GaN Power Amplifier MMIC Utilizing Combination of the Distributed and Reactive Matching Topology*," *2019 14th EuMIC*, 2019, pp. 228-231, doi: 10.23919/EuMIC.2019.8909556.